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Description

SYSTEM AND METHOD FOR SYNCHRONIZING DIVIDE-BY COUNTERS

BACKGROUND OF INVENTION

[0001] FIELD OF THE INVENTION

[0002] The present invention generally relates to the field of integrated circuits. More particularly, the present invention is directed to a system and method for synchronizing multiple divide-by counters with one another.

[0003] BACKGROUND OF THE INVENTION

[0004] Trends toward mobile and wireless computing and other power-sensitive applications utilizing various integrated circuit (IC) chips have created a need for multi-power-mode ICs that can operate in relatively low power mode when full processing speed is not needed. One approach for decreasing the dynamic power consumption of an IC is to slow down its functional clock(s). One way to slow down such clocks is to scale the clock frequency dynamically using a divide-by counter to generate one or more signals that each have a frequency that is a fraction of the full-power frequency. Each of these fractional, or divide-by, frequency clock signals may then be used during a low-power mode.

[0005] For operations such as system frequency scaling, voltage scaling and communications, it is necessary that systems containing multiple divide-by counters have their counters synchronized with one another. However, a synchronization problem arises at startup due to the initial states of the divide-by counters being unknown. A conventional solution to synchronizing multiple divide-by counters would be to synchronize the counters to a system clock. This solution, however, is not satisfactory when the clock signal experiences a clock mesh delay, i.e., the delay caused by the clock mesh between each divide-by counter and the clocked functional latches, is greater than the cycle time of the corresponding clock. This is so because across the various frequencies of the multiple clock domains, the individual counters could be reset to different clock cycles since the respective signals are in separate domains. Accordingly, there is a need for a system and method for synchronizing multiple divide-by counters across multiple clock domains.

SUMMARY OF INVENTION

[0006] In one aspect, the present invention is directed to an integrated circuit comprising a clock divider circuit that includes a counter operatively configured to generate a plurality of first signals from a second signal. Each one of the plurality of first signals has a first phase, and the second signal has a second phase. A mux is in electrical communication with the counter and is operatively configured to output a selected one of the plurality of first signals. A phase detector is operatively configured to detect an offset between the first phase of the selected one of the plurality of first signals and the second phase of the second signal and output a third signal

representing the offset.

[0007] In another aspect, the present invention is directed to a method of resetting at least one divide-by counter having an input signal with a first phase, the divide-by counter outputting a plurality of divide-by signals each having a second phase. The method comprises the steps of selecting one of the plurality of divide-by signals and determining a phase offset between the second phase of the selected one of the plurality of divide-by signals and the first phase of the input signal. The divide-by counter is then reset based upon the phase offset.

BRIEF DESCRIPTION OF DRAWINGS

[0008] For the purpose of illustrating the invention, the drawings show a form of the invention that is presently preferred. However, it should be understood that the present invention is not limited to the precise arrangements and instrumentalities shown in the drawings, wherein:

[0009] FIG. 1 is a high-level schematic diagram of a multiprocessor system wherein each processor includes a divide-by counter synchronization system according to the present invention;

[0010] FIG. 2A is a schematic diagram of the divide-by counter/mux systems of the processors of FIG. 1; FIG. 2B is a diagram illustrating the manner in which the divide-by counter of FIG. 2A generates divide-by frequencies;

[0011] FIG. 3 is a flow diagram for a method of synchronizing multiple divide-by counters with one another in accordance with the present invention; and

[0012] FIG. 4 is a timing diagram illustrating the states of Psync, Sysclk and Lclk

signals of FIG. 1 before, during and after synchronization and illustrating the four possible offsets of Mclk/4 signal of FIG. 1 prior to initiation of synchronization.

DETAILED DESCRIPTION

[0013] Referring now to the drawings, FIG. 1 shows in accordance with the present invention a multi-processor system, which is generally denoted by the numeral 100. System 100 may include any number of processors, e.g., processor A and processor B, each having functional circuitry 102_A, 102_B grossly timed by a common system clock 104. It is noted that two processors A, B are shown merely for the sake of simplicity and convenience in describing the invention. Those skilled in the art will readily understand the changes necessary to implement the present invention with any number of processors. Each processor A, B may be contained on separate chips or may be integrated into a single chip, e.g., within a system-on-chip type IC. Processors A, B may communicate with one another and/or external circuits/devices (not shown) via one or more communication links (not shown). Detailed descriptions of such communication links and external circuits/devices are not necessary for those skilled in the art to understand the broad scope of the present invention and how to practice the invention to its full scope.

[0014] Each processor A, B may contain, among other things, a PLL 108_A, 108_B that locks onto a Sysclk signal 112 generated by system clock 104. PLL 108_A, 108_B may be any type of conventional PLL used for generating a clock signal, i.e., PLLclk signal 116_A, 116_B. Those skilled in the art will

readily understand how to make a suitable PLL 108_A, 108_B such that a detailed description of the PLL is not necessary for those skilled in the art to practice the present invention. PLLclk signal 116_A, 116_B is provided to a counter/mux (multiplexer) system 120_A, 120_B, which is shown in more detail in FIG. 2A.

[0015] Referring to FIG. 2A, each counter/mux system 120_A, 120_B comprises a divide-by counter 124_A, 124_B, e.g., a count-up type counter, that includes a number of latches 128A, 128B for dividing the frequency of PLLclk into various divide-by frequencies, e.g., Mclk/1, Mclk/2, Mckl/4 . . . Mclk/64 . . . Mclk/n, where $n = 2^x$, where x is any integer equal to or greater than zero. Accordingly, the number of latches 128_A, 128_B needed for each divide-by counter 124_A, 124_B corresponds to the smallest divide-by frequency desired. For example, if the lowest desired frequency is one-sixty-fourth of the frequency of PLLclk signal 116A (i.e., Mclk/64 signal), counter 124_A would require at least six latches 116_A. The outputs of latches 116_A, 116_B of each counter 124_A, 124_B are input into a corresponding mux 132_A, 132_B, which permits the selection of the one of the divide-by Mclk/n signals to be provided to functional circuitry 102_A, 102_B (FIG. 1). For example, if functional circuitry 102_A, 102_B must be in a full-power mode, Mclk/1 signal 136_A, 136_B, i.e., the full frequency of PLLclk signal 116_A, 116_B, may be selected via mux 132_A, 132_B and thereby provided to the functional circuitry. On the other hand, if a low-power mode is considered to be a situation wherein functional circuitry 102_A, 102_B is clocked at one-sixty-fourth of the frequency of PLLclk signal 116A, 116B, then Mclk/64 signal 140_A, 140_B may be selected during the low-power mode via mux and

thereby provided to the functional circuitry.

[0016] FIG. 2B illustrates the manner in which latches 128_A, 128_B of each counter 124_A, 124_B of FIG. 2A generate the various frequencies of the corresponding divide-by frequency Mclk/n signal 144_A, 144_B. When counter 124_A, 124_B is a count-up type counter, after the counter is reset it counts from zero to its maximum (i.e., every latch containing a 1) in repeating manner until PLLclk signal 116_A, 116_B is no longer provided. For example, when counter 124_A, 124_B is a six-bit counter capable of providing a Mclk/64 signal, it repeatedly counts by ones from 0_{10} (000000_2) to 127_{10} (111111_2). The 2^0 latch changes state at one-half the frequency of PLLclk signal 116_A, 116_B to generate Mclk/2 signal, the 2^1 latch changes state at one-quarter the frequency of PLLclk signal to generate Mclk/4 signal, the 2^2 latch changes state at one-eighth the frequency of PLLclk signal to generate Mclk/8 signal, and so on.

[0017] Referring again to FIG. 1, each set of functional circuitry 102_A, 102_B may contain the logic, communications, memory and/or other circuitry that provides the corresponding processor A, B with its functionality. Those skilled in the art will understand that a detailed description of functional circuitry 102_A, 102_B is not necessary herein, since it may be any such circuitry routinely designed within the art for a particular application. That said, functional circuitry 102_A, 102_B may be generally characterized as having a plurality of latches 160_A, 160_B that are clocked by Mclk/n signal 144_A, 144_B output from counter/mux system 120_A, 120_B. Once Mclk/n signal 144_A, 144_B is output from counter/mux circuitry 120_A, 120_B, it reaches

latches 160_A, 160_B via a clock mesh 164_A, 164_B, which typically include a plurality of buffers (not shown), e.g. inverters, and wires (not shown) that branch down to the individual latches. Clock mesh 164_A, 164_B may be any conventional or other clock mesh. Clock mesh 164_A, 164_B causes a delay, primarily due to the length of wiring and buffers through which Mclk/n signal 144_A, 144_B must travel between counter/mux system 120_A, 120_B and latches 160_A, 160_B. Of course, the greatest delay will be present at the one (s) of latches 160_A, 160_B where Mclk/n signal 144_A, 144_B must travel through the longest wiring path and/or most buffers. Depending upon the frequency of sysclk signal 112 and the PLL multiplication factor, the delay in clock mesh 164_A, 164_B may be longer than one cycle of PLLclk signal 116_A, 116_B. As discussed in the background section above, such a long delay through clock mesh 164_A, 164_B complicates synchronizing divide-by counters 124_A, 124_B (FIG. 2A) of processors A, B with one another.

[0018] Referring to FIGS. 1, 2A, 3 and 4, FIG. 3 illustrates a method 200 of synchronizing divide-by counters 124_A, 124_B of processors A, B with one another regardless of the amount of the delay in Mclk/n signal 144_A, 144_B due to clock mesh 164_A, 164_B. It is noted that method 200 is described particularly with respect to Mclk/4 signal 168_A, 168_B, which, as discussed above, has a frequency of one-quarter the frequency of PLLclk signal 116_A, 116_B. As will be appreciated, method 200 can be extended to any of divide-by signals having a frequency smaller than the frequency of Mclk/4 signal 168_A, 168_B. This extension is discussed below, following the description of method relative to Mclk/4 signal 168_A, 168_B.

[0019] In general, method 200 begins in step 210 by simulating the delay that is caused by clock mesh 164_A, 164_B in a signal, e.g., Mclk/1 signal 136_A, 136_B, which may be the same as PLLclk signal 116_A, 116_B, so as to generate a delayed Lclk signal 172_A, 172_B having the same delay as Mclk/4 signal 168_A, 168_B after it propagates through clock mesh 164_A, 164_B. Delay may be introduced into Mclk/1, signal 136_A, 136_B via delay circuitry 176. Sysclk signal 112 and Mclk/4 signal 168_A, 168_B are input into a phase detector clocked by the Lclk signal 172_A, 172_B that detects whether or not the Mclk/4 signal is out of phase with the Sysclk signal 112. The reason Mclk/4 signal 168_A, 168_B may be out of phase with Sysclk signal 112 is that, as mentioned in the background section above, when divide-by counters 124_A, 124_B startup, the state of each latch 128_A, 128_B is unknown, i.e., may be either a 0 or a 1. Mclk/4 signals 168_A, 168_B may be out of phase depending upon the states of latches 128_A, 128_B corresponding to the two least significant bits of counter, i.e., 2^0 and 2^1 latches 148, 152 (FIG. 2B).

[0020] At step 220, synchronization may be initiated at time T_{init}. using a Psync signal 184, e.g., a single pulse signal. For example, during a pulse 188 of Psync signal 184 and at a rising edge 192 of Sysclk signal 112, at step 230 phase detector 180_A, 180_B will take two measurements of Mclk/4 signal 168_A, 168_B during the next two cycles of Lclk signal 172_A, 172_B. The values of these two measurements will determine the amount that Mclk/4 signal 168_A, 168B is shifted relative to Sysclk signal 112. Referring particularly to FIG. 4, it is seen that there are four possible states of phase difference between both Mclk/4 signals 168_A, 168_B, a 0 phase shift (i.e., in phase), a -

3 phase shift (i.e., 90°lagging), a -2 phase shift (i.e., 180° lagging) and a -1 phase shift (i.e., 270° lagging). As will become apparent after reading the description below, the phase shift designations "0," "-1," "-2" and "-3" refer to the base ten number that must be subtracted from corresponding divide-by counter 124_A, 124_B (FIG. 2A) in order to reset that counter so that Mclk/4 signals 168_A, 168_B are in phase.

[0021] With continuing reference particularly to FIG. 4, it is seen that if Mclk/4 signal 168A, 168B is in phase with Sysclk signal 112 (0 phase shift), the two measurements of the Mclk/4 signal following initiation of phase detection will be 1, 1 since the Mclk/4 signal is high during both of the two cycles of the Lclk signal following initiation of phase detection. Similarly, if Mclk/4 signal 168_A, 168_B is 90° lagging relative to Sysclk signal 112 ("-3" phase shift), the two measurements of the Mclk/4 signal will be 0, 1 since the Mclk/4 signal switches from low to high during the two measurement cycles of the Lclk signal. If Mclk/4 signal 168_A, 168_B is 180° lagging relative to Sysclk signal 112 ("-2" phase shift), the two measurements of Mclk/4 signal will be 0, 0 since the Mclk/4 signal is low during the two measurement cycles of the Lclk signal. Lastly, if Mclk/4 signal 168_A, 168_B is 270° lagging relative to Sysclk signal 112 ("-1" phase shift), the two measurements of the Mclk/4 signal will be 1, 0 since the Mclk/4 signal switches from high to low during the two measurement cycles of the Lclk signal.

[0022]
Once phase detector 180_A, 180_B detects the phase difference between Mclk/4 signal 168_A, 168_B and Sysclk signal 112, at step 240, the phase

detector may send an offset signal 194_A, 194_B to counter re-setter 196_A, 196_B that may be configured to (re)set the corresponding divide-by counter 124_A, 124_B to zero at step 250. Offset signal 194_A, 194_B may be an asynchronous signal containing information that allows re-setter 196_A, 196_B to reset divide-by counter 124_A, 124_B to zero. Referring particularly to FIG. 2B, it can be seen that measurements by phase detector 180_A, 180_B of Mclk/4 signal 168_A, 168_B can be related to the state of 2^1 latch 152 as divide-by counter 124_A, 124_B (FIG. 2A) counts. These measurements can also be related to the states of 2^1 and 2^0 latches 152, 148 at the time phase detection was initiated at time T_{init}. (FIG. 4).

[0023] That is, when Mclk/4 signal 168_A, 168_B is in phase with Sysclk signal 112 such that the two measurements are 1, 1, it can be seen from FIG. 2B that in the very next cycle of divide-by counter 124_A, 124_B following the two cycles of the counter wherein the states of 2^1 latch 152 are 1, 1, the states of 2^1 and 2^0 latches 152, 148 are 0, 0, respectively. Similarly, when the two measurements are 0, 1, i.e., Mclk/4 signal 168_A, 168_B is 90° lagging with respect to Sysclk signal 112 ("-3" phase shift), the states of 2^1 and 2^0 latches 152, 148 in the very next cycle of divide-by counter 124_A, 124_B following the two consecutive cycles of the counter wherein the states of 2^1 latch 152 are 0, 1, and 1, 1, respectively. Accordingly, to reset divide-by counter 124_A, 124_B so that 2^1 and 2^0 latches 152, 148 each contain a "0", effectively, the number 3_{10} must be subtracted from the counter, which would contain the number 3_{10}, i.e., $(11)_2$, if the counter were not reset.

[0024]

Similar determinations may be made for the phase differences of 180°and

270° lagging. For 180° lagging ("-2" phase shift), the states of 2^1 and 2^0 latches 152, 148 are 1, 0, respectively, in the cycle following the two cycles wherein the state of the 2^1 latch 152 is, consecutively, 0, 0. Accordingly, to reset 2^1 and 2^0 latches 152, 148 of divide-by counter 124_A, 124_B to zero, effectively, the number 2_{10} must be subtracted from the counter, which would contain the number 2_{10}, i.e., $(10)_2$, if the counter were not reset. Finally, for 270° lagging ("-1" phase shift), the states of 2^1 and 2^0 latches 152, 148 are 0, 1, respectively, in the cycle following the two cycles wherein the state of the 2^1 latch 152 is, consecutively, 1, 0. Accordingly, to reset 2^1 and 2^0 latches 152, 148 of divide-by counter 124_A, 124_B to zero, effectively, the number 1_{10} must be subtracted from the counter, which would contain the number 1_{10}, i.e., $(01)_2$, if the counter were not reset.

[0025] Divide-by counters 124_A, 124_B of processors A, B may be reset as described above. As can be appreciated, as long as any delays inherent in phase detectors, counter re-setter and associated wiring are the same for processors A, B across all divide-by frequencies, divide-by counters of the two processors will reset to zero at the same time when synchronization is initiated on the same pulse of Psync 184 signal. That said, any unsuitable delay can be compensated for by clocking counter re-setter 196_A, 196_B, e.g., using sysclk signal or a separate pulsed reset signal to activate the counter re-setters at the same time.

[0026] As mentioned above, method 200 of resetting and synchronizing divide-by counters 124_A, 124_B based on Mclk/4 signal 168_A, 168_B can be readily extended to any divide-by frequency smaller than the one-quarter

frequency of the Mclk/4 signal. In performing method for any divide-by frequency less than the one-quarter frequency of Mclk/4 signal 168_A, 168_B, the primary difference from performing the method for the Mclk/4 signal will be in the number of phase offset states and, accordingly, the number of measurements that must be taken to determine the offset for resetting divide-by counter 124_A, 124_B. In general, the number of phase offset states will be equal to the value of "n" in the divide-by frequency in the corresponding Mclk/n signal 144_A, 144_B, and the number of measurements needed to determine the phase offset present in that Mclk/n signal will be equal to n/2. The remaining steps of method 200 will generally be the same as the steps for Mclk/4 signal $168_{A,}$ $168_{B.}$

[0027] While the present invention has been described in connection with a preferred embodiment, it will be understood that it is not so limited. On the contrary, it is intended to cover all alternatives, modifications and equivalents as may be included within the spirit and scope of the invention as defined above and in the claims appended hereto.